REMARKS

The applicants appreciate the Examiner's thorough examination of the Application and request reexamination and reconsideration of the Application in view of the following remarks.

Claims 34 and 36 stand rejected under 35 U.S.C. 101 as allegedly being directed to non-statutory subject matter. Applicants have adopted the Examiner's suggestion and have amended claim 34 to recite that the computer program is embodied on a computer readable medium. Support for this amendment can be found at page 23, line 28 to page 24, line 18. Since independent claim 34 clearly recites statutory subject matter, applicants respectfully request that the Examiner withdraw this rejection under 35 U.S.C. 101.

Claims 1, 2, 7-10, 12, 17, 22-31 and 33 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by U.S. Patent No. 4,829,236 to Brenardi et al. Claims 3-6, 13-16, 18-20 and 34-37 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Brenardi et al. Claim 11 stands rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Brenardi et al. in view of U.S. Patent No. 4,419,656 to Sloane. Claims 21 and 32 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Brenardi et al. in view of U.S. Patent No. 5,818,370 to Sooch.

Applicants herein amend claims 1, 17, 21-23, 26 and 31-33 to better define the invention. Support for the amendments to claims 1, 17, 21-23 and 32-33 can be found at page 19, lines 12-27 and Fig. 6. Support for the amendments to claims 26 and 31 can be found at page 5, lines 15-32 and page 20, lines 5-15. Applicants also amend claim 33 herein to correct a minor typographical error.

The subject invention results from the realization that a less complex, in an analog

sense, more robust compensation of a digital to analog converter may be effected by applying to the digital input to the DAC anti-function digital processor to precondition the digital input to compensate for the error function of the DAC and provide non-linear error compensation. The subject invention results from the further realization that those digital coefficients can be generated by measuring the output of the DAC with known inputs, determining the error function of the DAC from the measured outputs, and combining the error function with a suitable mathematical expression to generate the anti-function digital coefficients. The mathematical expression, known as a basis function, is selected such that the generated anti-function digital coefficients can provide non-linear error compensation. The basis function may be selected from a plurality of basis functions to provide the most suitable error compensation.

A variety of digitized basis functions can be used to create the anti-(error) function for compensating for DAC transfer function errors. There are a large variety of digitized basis functions known in the art of mathematics or which can be derived from mathematical textbooks, for example `Linear System Theory`, W. J. Rugh, 2.sup.nd Edition, Prentice Hall 1996. Orthogonal basis functions may also be used to describe signals and one of the most commonly used orthogonal basis functions is Fourier series and the Fourier transform and Fast Fourier Transform (FFT) techniques are in ubiquitous use for real-world time/frequency domain signal analysis. For digital signals, Radamacher functions or Walsh functions are more applicable. *See* the subject application at page 5, line 15 to page 6, line 17.

Brenardi et al. relates to a digital to analog calibration system that uses stored calibration characteristics to adjust digital data. Brenardi et al., however, relies solely on

a single application of the equation y=mx+b to adjust digital data over the entire range of the digital to analog converter. The single application use of this equation over the entire input range severely restricts the ability of the Brenardi et al. apparatus to adequately compensate for the error of the DAC. By using the linear equation y=mx+b in the manner that it does, Brenardi et al. apparatus can only compensation for linear errors that follow this equation.

In contrast to Brenardi et al., the subject invention compensates for non-linear errors. The applicants use of a non-linear anti-error function is best seen in Fig. 6 which illustrates how accurately the subject invention can compensate for non-linear DAC or ADC errors. By applying generated anti-function digital coefficients to the digital input of a digital to analog converter, the subject invention as claimed by applicants not only digitally compensates for the error function of the digital to analog converter, it provides non-linear error compensation. The Brenardi et al. apparatus cannot provide this functionality.

Moreover, since a variety of digitized basis functions can be used to create the anti-function for compensating for DAC transfer function errors, the subject invention may select a basis function from a plurality of basis functions to obtain the most suitable error compensation. Also, various implementations of the anti-function generator are possible depending on which basis function is selected. *See* the subject application at page 20, lines 5-15.

Claim 1 of the subject invention recites: "A digitally compensated digital to analog converter system comprising: a digital to analog converter; a storage device for storing anti-function digital coefficients corresponding to an error function of the digital

to analog converter; and an anti-function processor for applying generated anti-function digital coefficients to the digital input of the digital to analog converter for digitally compensating for the error function of the digital to analog converter, said anti-function digital coefficients providing non-linear error compensation."

As noted above, Brenardi et al. fails to teach, disclose or suggest applicants' claimed digitally compensated digital to analog converter system that provides non-linear error compensation. Independent claims 17, 21-23 and 32-33 recite similar features that distinguish over Brenardi et al.

Moreover, as noted above, Brenardi et al. fails to teach, disclose or suggest applicants' claimed method of generating anti-function digital coefficients for a digital to analog converter that includes the step of selecting a digital basis function from a plurality of digital basis functions, as recited in applicants' independent claim 31.

Accordingly, Applicants respectfully request that the Examiner withdraw the rejections of independent claims 1, 17, 21-23 and 32-33 and the claims depending therefrom under 35 U.S.C. §102(b) and 35 U.S.C. §103(a).

If for any reason this Response is found to be incomplete, or if at any time it appears that a telephone conference with counsel would help advance prosecution, please telephone the undersigned, or his associates, collect in Waltham, Massachusetts, at (781) 890-5678.

Respectfully submitted,

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